DRAWINGS

The attached sheet of replacement drawings is submitted in compliance with 37 C.R.F. § 1.121(d) to replace the original sheet containing FIG. 1 to correct anomalies.

Attachment: One Replacement Sheet.

REMARKS

It is believed that the above amendments and following remarks attend to each and every rejection and objection presented in the December 19, 2005 Office Action.

Claim 4 is amended to spell-out the acronym "HLSN" as "highest level signal name". No new matter is added.

Claims 1-20 remain pending, with claims 1, 16, 19 and 20 being independent.

Drawing Objections

The drawings stand objected to because the connection from processor 112 to storage unit 106 is misplaced, as is connection 111 between sources 110 and processor 102 and the connection between output unit 108 and processor 102. A replacement sheet containing FIG. 1 is attached, in compliance with 37 CRF § 1.121(d). FIG. 1 is amended to correct these connections between processor 112, sources 110, storage unit 106 and output unit 108. Reconsideration is respectfully requested.

Specification Amendment

Paragraph [0001] is amended to replace attorney docket numbers with U.S. patent application numbers for copending, co-filed applications.

No new matter is added.

Claim Objections

Claims 1, 4, 16, 19 and 20 stand objected to because of informalities. Regarding the objections to claims 1, 16, 19 and 20, we respectfully disagree.

The Examiner objects to the term "entity in a design portion of interest in the circuit design" as used in claims 1, 16, 19 and 20. Paragraph [0015] of the specification teaches that "an 'entity' is for example any part of a circuit design 109, such as a design element, group of design elements, HLSN, net, net piece, cell, and block; and entity may also be a group of such entities." Paragraph [0019] teaches that "each data source indicator 103(*) is a 'bit vector' in which, for example, each bit in the vector indicates the source 110(*) of the data used for, or applicable to, one or more ***entities of interest in design 109***." *{Emphasis added}* Paragraph [0020] teaches that "when analysis of an HLSN, block, or other ***portion of design 109*** is complete, a

determination is made in step 215 as to whether data source indicators 103(*) are to be saved for later use by another analysis tool." *{Emphasis added}* Since only a portion of a circuit design need be analyzed, clearly only entities within that portion are of interest. We therefore believe the phrase "entity in a design portion of interest in the circuit design" is clear; we thus request reconsideration.

The Examiner also objects to the phrase "indicia applicable to the entity." Paragraph [0019] of the specification teaches that "combinations of bits within a data source indicator 103(*) may be used as ***indicia*** to represent one or more data sources or to represent additional information, such as the type of analysis performed, limits that were applied to numeric quantities, or errors that occurred while processing the design element." *{Emphasis added}* Since, as noted above, an entity is a part of a circuit design, the term 'indicia applicable to the entity' identifies one or more indicators applicable to a particular entity within the circuit design.

Reconsideration of claims 1, 4, 16, 19 and 20 is respectfully requested.

Claim Rejections – 35 U.S.C. §102

Claims 1-20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication Number US2003/0005394 A1 of Buchanan (hereinafter "Buchanan"). Respectfully we disagree.

In view of the Examiner's reasons for rejecting claims 1-20 over Buchanan, it appears to us that the Examiner has misunderstood the terms 'data source' and 'bit vector' as claimed. It is therefore hoped that the following overview will help clarify differences between the immediate application and Buchanan.

The immediate application teaches of a method of identifying a source of data used in an analysis of a portion of a circuit design. A bit vector is, for example, utilized to encode the data source information and may be processed to generate formatted output. As disclosed in paragraph [0019] of the specification, each data source indicator 103(*) is a 'bit vector' in which each bit indicates the source 110(*) of the data used for analysis of one or more entities of interest in design 109. Thus, an entity has an associated data source indicator, each bit of which indicates a source of data used during analysis of the entity. These data source indicators may be stored in a file along with analysis results for use by another analysis tool. See paragraph [0020]

of the specification. Thus, when used by another analysis tool, the results indicate relevant data sources used in generation of the results. The immediate application teaches that indicia of data sources used during an analysis may be encoded with results from the analysis.

On the other hand, Buchanan discloses a method for evaluating design code of an integrated circuit by assigning an identifier to a cell, based upon characteristics of the cell, and then associating the identifier or characteristics with a cell embedded within the design code. See Buchanan abstract. Buchanan does not disclose or suggest encoding identities of data sources to provide data used during analysis of an entity of the circuit design. Buchanan discloses characteristics of a cell; but these characteristics do not identify data sources for the cell. That is, the characteristics of Buchanan relate to the design of the cell, and do not provide indication of data sources used during analysis of the cell. Buchanan also discloses an identifier; but this identifier is generated and assigned to a cell. See Buchanan paragraph [0047]. Thus, the identifier of Buchanan functions only as a 'label' for the cell. Buchanan does not disclose identifying sources of data, or utilizing bits of a 'bit vector' to identify data sources.

In particular, claim 1 recites a method for identifying data sources associated with a circuit design, including:

a) retrieving data source information including identification of a data source used to generate data for an entity in a design portion of interest in the circuit design;

b) formatting the data source information as a bit vector associated with the entity, wherein each of a plurality of bits in the bit vector comprises indicia applicable to the entity; and

c) processing the bit vector to generate formatted output.

Step a) of claim 1 recites that identification of a data source used to generate data for an entity in a design portion of interest in the circuit design is retrieved. That is, a data source that generates data for an entity of a circuit design is identified. As disclosed by paragraph [0016] of the specification, data sources may include user input, design analyzers, computer aided design tool data estimators, and the like. Step

a) thus retrieves information from the data source, including identification of the data source.

Buchanan discloses associating records with cell characteristics, where the characteristics 'may regard the origin of the cell, such as its creation date or parent library.' See Buchanan paragraph [0018]. But, Buchanan does not disclose or suggest retrieving information of a data source that ***generates data*** for an entity of the circuit design. The 'characteristics' of Buchanan are not equivalent to 'data source information' of claim 1. In the immediate application, the source of data used during analysis of the entity is, for example, stored within a bit vector, and not the design information for the entity.

Step b) of claim 1 recites that the data source information be formatted as a bit vector associated with the entity, wherein each of a plurality of bits in the bit vector comprises indicia applicable to the entity. The Examiner quotes paragraph [0033] of Buchanan as anticipating step b) of claim 1 and asserts that a 'sequence' of bits in the design file is equivalent to a bit vector. However, Buchanan make no disclosure that a sequence of bits from the design file is used as a bit vector; the Examiner makes this assumption without supporting disclosure within Buchanan. As disclosed in paragraph [0019] of the immediate specification, "each bit in the vector indicates the source 110(*) of the data used for, or applicable to, one or more entities of interest of the design." Buchanan does not disclose such use of bits within a bit vector.

Step c) of claim 1 recites that the bit vector is processed to generate formatted output. The Examiner asserts that paragraphs [0034] and [0058] of Buchanan anticipate step c). However, Buchanan does not disclose – anywhere - processing a bit vector to generate formatted output. As taught by paragraphs [0022] – [0025], table 1 and output table 111 of the immediate specification, each bit of the data source indicator may be processed for output as indicated by the example of paragraph [0024]. Buchanan does not disclose processing a bit vector to generate formatted output. In fact, Buchanan, in paragraph [0058], discloses that "the embodiment may output identifiers associated with located characteristic fields." Outputting of identifiers is not the same as processing a bit vector to generate formatted output.

For at least these reasons, Buchanan cannot anticipate claim 1. Reconsideration of claim 1 is respectfully requested.

Claims 2-15 depend from claim 1 a benefit from like argument. However, these claims have other features that patentably distinguish over Buchanan. For example, claim 2 recites that the entity is at least one design element in the design portion of interest. Claim 3 recites that the entity is a group of design elements in the design portion of interest. Claim 4 recites that the entity is a highest level signal name in the design portion of interest. Claim 5 recites that the entity is a net in the design portion of interest. Buchanan does not disclose such features, and operates only upon 'cells'.

Claim 6 recites that the indicia includes information that identifies at least one specific data source applicable to the entity. As argued above, Buchanan does not disclose identifying a data sources, or disclose indicia for identifying the data source.

Claim 7 recites retrieving information that identifies a type of analysis performed by the CAD tool, and that the indicia identifies a specific type of the analysis. The Examiner asserts that the file formats GDS or CIF represents the step of retrieving information that identifies a type of analysis. However, the GDS and CIF files contain definitions of circuitry, and not indicia of data sourced used during an analysis of the circuit design.

Claim 8 recites retrieving data source information that identifies limits that were applied to numeric quantities in the analysis, and that the indicia identifies the limits. Buchanan does not disclose indicia identifying limits. In fact, Buchanan does not disclose - anywhere - limits being applied to numerical quantities. In paragraph 14 of the pending office action, the Examiner cites paragraphs [0066]-[0068] of Buchanan as anticipating claim 8. However, the relevance of these cited paragraphs to claim 8 (and in particular to limits applied to numerical quantities) is not understood; we find no such disclosure within Buchanan.

Claim 9 recites retrieving data source information that identifies errors that occurred while processing a design element, and that the indicia identifies the errors. In paragraph 15 of the pending office action, the Examiner asserts that an identifier corresponding to a defective cell within Buchanan anticipates claim 9. However, Buchanan does not disclose processing a design element as required by claim 9. In paragraph [0055] of Buchanan, the designer may type in or otherwise indicate the

identifier that corresponds to a defective cell. The identifier of Buchanan is not equivalent to data source information.

Claim 10 recites displaying the bit vector. In paragraph 16 of the pending office action, the Examiner asserts that to recall an identifier from a database anticipates claim 10. Recalling data from a database does not mean that the identifier is displayed. Further, as noted above, the identifier is not a bit vector.

Claim 11 recites storing the bit vector in a file. As argued above, the identifier is not a bit vector and thus the action of Buchanan to store the identifier within a database does not anticipate claim 11.

Claim 12 recites that the bit vector is overloaded such that a specific subset of a plurality of bits therein has a significance dependent on the specific subset and on usage context of the bit vector. However, paragraph [0040] of Buchanan, as cited by the Examiner in paragraph 18 of the pending office action, relates to generating a signature for a cell. Buchanan makes no disclosure of a bit vector, let alone of overloading the bit vector. Signature generation does not relate to overloading a bit vector; we believe that Buchanan paragraph [0040] is not pertinent. Clarification is respectfully requested should the Examiner maintain this rejection.

Claim 13 recites that the indicia identifies a specific type of the analysis. Buchanan does not disclose indicia for identifying a specific type of analysis.

Claim 14 recites that the indicia identifies limits that were applied to numeric quantities in the analysis. Buchanan does not disclose indicia that identify limits applied during an analysis.

Claim 15 recites that the indicia identifies errors that occurred while processing a design element in the design portion of interest. Buchanan does not disclose indicia that identify errors that occurred during processing of a design element.

For at least these reasons, Buchanan does not anticipate claims 2-15. Reconsideration of claims 2-15 is respectfully requested.

Claim 16 recites a system for identifying a data source used by a CAD tool in analysis of a circuit design, wherein a plurality of data sources are available to the CAD tool, including:

a) a processor coupled to a computer memory;

b) a plurality of data source indicators, stored in the computer memory, each of which comprises a plurality of bits for identifying the data sources associated with an entity in a design portion of interest in the circuit design; and

c) a table, stored in the computer memory, for formatting the data source indicators.

Step b) of claim 16 recites that each of a plurality of data source indicators has a plurality of bits for identifying the data sources associated with an entity in a design. As argued above, Buchanan does not disclose data source indicators, and therefore cannot disclose that each data source indicator has a plurality of bits that indicate sources of data associated with an entity within the circuit design. Step c) of claim 16 recites a table within computer memory for formatting the data source indicators. Buchanan does not disclose a table for formatting data source indicators.

For at least these reasons, Buchanan cannot anticipate claim 16. Reconsideration of claim 16 is respectfully requested.

Claims 17 and 18 depend from claim 16 and benefit from like argument. However, these claims have additional features that patentably distinguish over Buchanan. For example, claim 17 recites that the data source indicators are generated from information retrieved from the data sources. Buchanan does not disclose data source indicators that are generated from data retrieved from the data sources. Claim 18 recites that a plurality of the bit vectors are processed by the processor to generate formatted output. Buchanan does not disclose processing bit vectors to generate formatted output.

For at least these reasons, Buchanan cannot anticipate claims 17 and 18. Reconsideration of claims 17 and 18 are respectfully requested.

Claim 19 recites a system for identifying data sources associated with a circuit design, including:

a) means for retrieving data source information that identifies at least one of the data sources;

b) means for formatting the data source information as a bit vector, wherein each of a plurality of bits in the bit vector comprises indicia of a specific data

source applicable to an entity in a design portion of interest in the circuit design; and

c) means for processing the bit vector to generate formatted output.

Step a) of claim 19 recites retrieving data source information that identifies at least one of the data sources. Buchanan does not disclose retrieving data source information. The 'characteristics' of Buchanan are not equivalent to 'data source information' of claim 19. The identifier of Buchanan is not equivalent to the data source information of claim 19. As disclosed by paragraph [0018] of the specification, the data source information is relevant to the source of data used during analysis of the entity.

Step b) of claim 19 recites formatting the data source information as a bit vector, wherein each of a plurality of bits in the bit vector comprises indicia of a specific data source applicable to an entity in a design portion of interest in the circuit design. As argued above, the design file of Buchanan, whether it is in binary format or not, is not equivalent to a bit vector.

Step c) of claim 19 recites processing the bit vector to generate formatted output. As argued above, Buchanan does not disclose processing a bit vector to generate formatted output.

For at least these reasons, Buchanan cannot anticipate claim 19. Reconsideration of claim 19 is respectfully requested.

Claim 20 recites a software product having instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for identifying data sources used in analysis of a circuit design, including:

a) instructions for retrieving data source information that identifies a data source;

b) instructions for formatting the data source information as a bit vector, wherein each of a plurality of bits in the bit vector comprises indicia of the data source applicable to an entity in a design portion of interest in the circuit design; and

c) instructions for processing the bit vector to generate formatted output.

Step a) of claim 20 recites retrieving data source information that identifies at least one of the data sources. Buchanan does not disclose retrieving data source information. The 'characteristics' of Buchanan are not equivalent to 'data source information' of claim 20. The identifier of Buchanan is not equivalent to the data

source information of claim 20. As disclosed by paragraph [0018] of the specification, the data source information is relevant to the source of data used during analysis of an entity.

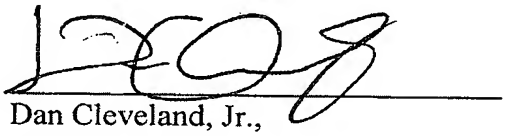
Step b) of claim 20 recites formatting the data source information as a bit vector, wherein each of a plurality of bits in the bit vector comprises indicia of a specific data source applicable to an entity in a design portion of interest in the circuit design. As argued above, the design file of Buchanan, whether it is in binary format or not, is not equivalent to a bit vector.

Step c) of claim 20 recites processing the bit vector to generate formatted output. As argued above, Buchanan does not disclose processing a bit vector to generate formatted output.

For at least these reasons, Buchanan cannot anticipate claim 20. Reconsideration of claim 20 is respectfully requested.

It is believed that no fees are due in connection with this amendment. If any fee is due, please charge Deposit Account No. 08-2025.

Respectfully submitted,

By: 

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